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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/034,227	12/28/2001	Timothe Litt	1662-53000 JMH (P01-3850)	9091

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 04/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,227	LITT, TIMOTHE	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,7-18,20-43,45,47,49-60 and 62-64* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7-18,20-43,45-47,49-60 and 62-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is a FINAL Office Action in response to AMENDMENT filed 3/15/2005.

Claims 1-64 were previously examined in the Prior Office Action, mailed 12/15/2004.

Claims 1, 3-7, 10, 14, 23, 31, 35, 43, 45, 46,49, 52, 56 have been amended.

Claims 2, 6, 19, 44, 48, 61 have been cancelled.

Claims 1, 3-5, 7-18, 20-43, 45, 47, 49-60, 62-64 are pending.

Prior Office Action art rejection is still maintained. Claims 1, 3-5, 7-10, 15-18, 20-35, 37, 39-43, 45-47, 49-52, 57-60 and 62-64 are rejected under 35 U.S.C. 102(e) as being anticipated by Arimilli et al. (U.S. Patent No. 6,633,838) and,

Claims 11-14, 36, 38, 53-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (U.S. Patent No. 6,633,838).

Response to Arguments

2. Applicant's arguments filed 3/15/2005 have been fully considered but they are not persuasive.

Reegarding independent Claims 1, 37, 43, as amended, Applicant argues that Arimilli does not anticipate the limitation of a "Boolean logic section which includes a plurality of software match logical units that detect a software event".

In response to Applicant's argument, Examiner notes that Arimilli discloses a Boolean logic section (Figures 4 and 5), which includes a plurality of bit-wise logical

(XNOR and OR) for performing comparison of event data from a variety of VLSI logic circuits with programmable pattern 405, 410 or 415, as disclosed by Arimilli, accordingly: " Specifically, event data from a variety of VLSI logic circuits is compared to at least one programmable pattern 405, 410 or 415, by a bit-wise logical XNOR of the event data and the pattern. The result of each bit-wise logical XNOR operation is then filtered through a programmable don t care mask, 420, 425, or 430, to exclude bits which are not of interest, by performing a bit-wise logical OR operation between the results of the XNOR operation and the don t care mask...., thereby producing a trigger". Arimilli, merely, uses well known in the art XNOR and OR logic symbols for designating comparison operations, which may be performed by software or hardware depending on test design requirements.

Clearly, Arimilli nowhere ever mentions or suggests that the comparison operation is performed by hardware as argued by the Applicant. Furthermore, Applicant himself admits that comparing is performed by an OR gate, as shown in Figure 5 of the invention, which illustrates a software matcher of Figure 2, comprising an OR gate 261 for comparing a match register input with a mask register input, and if detected by the software matcher, causes a true output at the output of OR gate 261.

In response to Applicant's argument, regarding Claim 23 as amended, Examiner notes Arimilli discloses a counting device (counter 670, Figure 6) to count the number of times, when a match condition occurs. As the trigger counter 670 is incremented, the count is compared 675 to a programmable count value 680. When the number of

triggers reaches the programmed value, the condition is met 685, which generates "RESET TRIGGER COUNTER" signal for loading the counter with a value.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 3-5, 7-10, 15-18, 20-35, 37, 39-43, 45-47, 49-52, 57-60 and 62-64 are rejected under 35 U.S.C. 102(e) as being anticipated by Arimilli et al. (U.S. Patent No. 6,633,838, filed: November 4, 1999, hereinafter, Arimilli).

Regarding independent Claim 1, Arimilli discloses an integrated circuit (VLSI circuit 100) fabricated on a chip, comprising: an on-chip logic analyzer (multi-state logic analyzer 120) including a word recognizer (condition select logic 150), Figure 1.

An on-chip memory (array 140) capable of storing data selected by the word recognizer (150), wherein the word recognizer (150) includes a Boolean logic section (logical XNOR and OR operation, Figures 4 and 5) and a counter/timer section including a (counter 670, Figure 6) located on-chip.

Arimilli further discloses a Boolean logic section (Figures 4 and 5), which further includes a plurality of software match logical units (XNOR and OR) using (programmable pattern 405, 410 or 415) and programmable don t care mask, (420, 425, or 430), which are capable of detecting a software event, and which produce a true output signal TRIGGER (435, 440, or 445). Furthermore, the Boolean logic section permits a user to enable one or more individual hardware match logical units (XNOR and OR) by controlling the event data from the trace data control logic 130 (as shown in FIG. 1).

Regarding independent Claim 23, Arimilli discloses a processor, such as integrated circuit (VLSI circuit 100) fabricated on a chip, including the pertinent limitations as applied in the independent claim 1, above.

Arimilli further discloses a counting device (counter 670, Figure 6) to count the number of times, when a match condition occurs. As the trigger counter 670 is incremented, the count is compared 675 to a programmable count value 680. When the number of triggers reaches the programmed value, the condition is met 685, which generates "RESET TRIGGER COUNTER" signal for loading the counter with a value.

Regarding independent Claim 37, Arimilli discloses a processor, such as integrated circuit (VLSI circuit 100) fabricated on a chip, including the pertinent limitations as applied in the independent claim 1, above. In addition, Arimilli discloses (Figures 4 and 5) a plurality of software match logical units (XNOR and OR) using (programmable pattern 405, 410 or 415) and programmable don t care mask, (420, 425, or 430), which are capable of detecting a software event, and which produce a

true output signal TRIGGER (435, 440, or 445). Furthermore, the Boolean logic section permits a user to enable one or more individual hardware match logical units (XNOR and OR) by controlling the event data from the trace data control logic 130 (as shown in FIG. 1).

Arimilli further discloses a Boolean logic section (Figures 4 and 5), which further includes a plurality of software match logical units (XNOR and OR) using (programmable pattern 405, 410 or 415) and programmable don t care mask, (420, 425, or 430), which are capable of detecting a software event, and which produce a true output signal TRIGGER (435, 440, or 445). Furthermore, the Boolean logic section permits a user to enable one or more individual hardware match logical units (XNOR and OR) by controlling the event data from the trace data control logic 130 (as shown in FIG. 1).

Regarding independent Claim 43, Arimilli discloses a word recognizer (condition select logic 150), which is fabricated on-chip as part of an integrated circuit (VLSI circuit 100), Figure 1, comprising:

A Boolean logic section (logical XNOR and OR operation, Figures 4 and 5), and a counter/timer section including a (counter 670, Figure 6), both located on-chip.

Arimilli further discloses a Boolean logic section (Figures 4 and 5), which further includes a plurality of software match logical units (XNOR and OR) using (programmable pattern 405, 410 or 415) and programmable don t care mask, (420, 425, or 430), which are capable of detecting a software event, and which produce a true output signal TRIGGER (435, 440, or 445). Furthermore, the Boolean logic section

permits a user to enable one or more individual hardware match logical units (XNOR and OR) by controlling the event data from the trace data control logic 130 (as shown in FIG. 1).

Regarding Claims 3,4, 45-46, Arimilli discloses a Boolean logic section (Figures 4 and 5), which includes a plurality of hardware match logical units (XNOR and OR) which are capable of comparing a match value with internal state data, and producing a true output signal if the comparison indicates a match condition, disclosed as follows:

The event data from a variety of VLSI logic circuits is compared by a bit-wise logical XNOR of the event data and the pattern. The result of each bit-wise logical XNOR operation is then filtered by performing a bit-wise logical OR operation. The bits resulting from the bit-wise logical OR operation are then passed through a bit-wise logical AND so that if all bits are 1, the logical AND will generate a 1, thereby producing a trigger. Any other combination of bits will not generate a trigger, thereby producing a trigger, (435, 440, or 445).

Regarding Claims 5, 47, Arimilli discloses a hardware match logical units (XNOR and OR), which produce a single bit output signal corresponding to trigger, (435, 440, or 445), and using triggers, 500, 505, 510, 515, 520, or 525, to a condition trigger mask 530 by a bit-wise logical AND, 535, 540, 545, 550, 555, or 560. The results of each logical AND operation are then passed through a bit-wise logical OR 565, so that if any trigger matches the condition trigger mask 530, the condition will be met 570, Figure 5.

Regarding Claims 7, 31, 32, 39, 49, Arimilli discloses a Boolean logic section (Figures 4 and 5), which further includes a plurality of software match logical units

(XNOR and OR) using (programmable pattern 405, 410 or 415) and programmable don t care mask, (420, 425, or 430), which are capable of detecting a software event, and which produce a true output signal TRIGGER (435, 440, or 445). Furthermore, the Boolean logic section permits a user to enable one or more individual hardware match logical units (XNOR and OR) by controlling the event data from the trace data control logic 130 (as shown in FIG. 1)

Regarding Claims 8, 33, 40, 50, Arimilli discloses output signals TRIGGER (435, 440, or 445, Figure 4) corresponding to triggers (500, 505, 510, 515, 520, or 525, Figure 5) of the hardware match logical units and the software match logical units connecting to AND (535, 540, 545, 550, 555, or 560, Figure 5) and an OR (565), and selecting on an whether the AND term or the OR term is enabled through condition trigger mask 530.

Regarding Claims 9, 10, 34, 35, 41, 42, 51, 52, Arimilli discloses logical units AND (535, 540, 545, 550, 555, or 560, Figure 5) with their output signals combined together in an OR term (565), so that if any trigger matches the condition trigger mask 530, the condition will be met 570, Figure 5.

Regarding Claim 15-18, 20, 24-28, 57-60, 62, Arimilli discloses a counting device (counter 670, Figure 6) to count the number of times, when a match condition occurs. As the trigger counter 670 is incremented, the count is compared 675 to a programmable count value 680. When the number of triggers reaches the programmed value, the condition is met 685, which generates "RESET TRIGGER COUNTER" signal for loading the counter with a value.

Regarding Claims 21, 22, 29, 30, 63, 64, Arimilli discloses an on-chip memory (array 140) for storing internal state data in response to the issuance of the Match signal, (CONDITION MET 685), and wherein the on-chip memory comprises cache memory.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 11-14, 36, 38, 53-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US 6633838), ISSUED: October 14, 2003, FILED: November 4, 1999 (hereinafter, Arimilli).

Regarding Claims 11, 36, 53, Arimilli does not explicitly disclose a multiplexer for selectively combining the output of the AND gate and the output of the OR gate. However, Arimilli discloses a bit-wise logical OR 565 gate which combines all the trigger output signals generated from the corresponding AND gate and OR gate logical units. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the bit-wise logical OR, as taught by Arimilli, for the purpose of combining all signals into one logical output. A person skilled in the art would have been motivated to use only one logical OR gate, since it is cost effective by avoiding the

implementation of unnecessary switching components, and further reducing the amount of I/O pins required associated with the implementation of additional switching components.

Regarding Claims 12, 13, 54, 55, Arimilli does not explicitly disclose a multiplexer output selectively coupled to a second multiplexer via two different signal paths, and wherein the first signal path remains asserted if a match condition exists, and the second signal path is asserted for the first clock period that the match condition exists. However, Arimilli discloses a bit-wise logical OR 565 gate which combines all the trigger output signals generated from the corresponding AND gate and OR gate logical units. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the bit-wise logical OR, as taught by Arimilli, for the purpose of combining all signals into one logical output. A person skilled in the art would have been motivated to use only one logical OR gate, since it is cost effective by avoiding the implementation of unnecessary switching components, and further reducing the amount of I/O pins required associated with the implementation of additional switching components.

Regarding Claims 14, 38, 56, Arimilli substantially discloses a counting device (counter 670, Figure 6), which can programmed by data control logic 130, which provides start, stop, run-n, stop-n, or reset commands to the trace data control logic depending upon the programming of the condition select logic. Arimilli does not explicitly disclose counting device that is capable of being programmed by a user to count the number of times a match condition occurs. However, the (counter 670,

Figure 6) disclosed by Arimilli is programmed by data control logic 130, which provides the control commands to the counter. Furthermore, it is well known in the art to use programmable automated or manual methods for the purpose of programming counters. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the automated control logic, as taught by Arimilli, to program (counter 670). A person skilled in the art would have been motivated to program a counter using an automated control method versus a manual method performed by a user, because the automated control method it is more reliable.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2133

By: _____

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PRIMARY EXAMINER

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